Projected status concerning x-ray detectors at the APS, 5 years out.

Written by Steve Ross ANL/APS/XSD/BTSG/skross@anl.gov, per instructions from Denny Mills, July 29, 2008.

This memo assumes people have access to a similar memo, March 14, 2008 Strengthening x-ray detector development and support efforts at the APS, from P. Fernandez given as input to APS Medium Term Proposal). That memo discusses more the "how to get there" aspects – strengthening APS detector development effort, expansion of detector test and modeling capabilities, expected user community, enabling technology and infrastructure. REF: http://www.aps.anl.gov/Renewal/Proposals/BTS_medium_term.pdf

This memo addresses the question of "Where could the APS be in x-ray detectors in five years?" and is thus more of a forecast of what detectors will be like in general in 5 years. For convenience I give [electronic response times] of the detector families.

These are simply my opinions.

In the past 5 years, we have seen:

- Successful commercialization of pixel array detectors (PAD's) from light sources such as Pilatus from SLS. [250 ns]
- Greater synchrotron use of detectors developed for medical imaging (amorphous silicon flat panels). [0.1 to 0.03 sec]
- Modest commercial expansion in the capabilities of energy dispersive detectors. For example companies that make silicon drift diodes now are a bit more flexible in what they offer, trying to produce modest arrays. [1us]
- The pushing to the limits of performance the venerable charge coupled device (CCD), with near column parallel readout and direct detection. [0.01 sec]
- At least at the APS, very modest use of application specific, customized detectors, such as strip detectors for arrays of energy dispersive elements, or counting. [microseconds]

One can make some predictions for 5 years from now (no particular order here….):

- Large format **CCD cameras** [1 sec] will continue in use, and will be sold almost entirely by commercial companies.
  - Their size will not grow much past 30-40 cm active area linear dimension; past that point their maintenance cost becomes high. Such things will cost approximately $1M.
  - Companies will seek to commercialize national lab progress in column parallel readout cameras, and in 5 years we might see 10 cm x 10 cm size 100 fps, direct detection cameras, for $1M.
- **CCD development** [0.1sec to 0.1ms] will focus on niche markets – small formats, customized pixel sizes, fast readout, and direct detection. Today it is not possible to buy a CCD, or a CCD camera with specifications, say, of pixel size 23 um x 180 um, array of 16 x 54, direct detection, frame rates of 300 frames per second. In 5 years

this arbitrary example CCD will like be more available "on-demand". A CCD wafer run costs about $200K, and if enough small jobs join together, a variety can be made on a 4" or 6" silicon wafer. Such wafer runs will be paid for by coordinating multiple synchrotron's needs and funds.

- Similarly **photodiode arrays** [1ms – 0.1 us] will be more custom format. In this case a 4" wafer run costs about $30K, again opening things up for many custom jobs. Photodiode arrays will generally be faster frame rate than CCD arrays, essentially just a fact of physics. However they will require application specific integrated circuits as readout, they cost $20K - $50K now. An example "funny" shaped array might be an array with a hole in the center for the beam to pass thru. We might see some use of germanium, or of high resistivity silicon used in a CMOS-like process.
- **Silicon drift diode** [1 us] arrays will start to appear quasi-commercially. Perhaps we see an 8 x 8 array of 300 um size diodes, each with 250 eV energy resolutions in a few microseconds. It seems that arrays larger than this may suffer from yield problems, but if people can live with this, then array size can grow much more. Why not a 100 x 100 SDD array, where 90% of them function? The cost will drop to the range of <$1K per channel, with pro-rated economies of scale.
- Improvements will be made to **PAD detectors**. [1us to 1ns] They will become the dominant detector architecture for high end applications.
  - They will become faster (dropping from 200 ns/ sample to perhaps 10 ns/sample. Their readout time will fall by a factor of 5 – 10 (from several milliseconds to several hundred microseconds).
  - There will be increased circuitry or logic under each pixel, perhaps by use of so-called 3-D CMOS, essentially layers of planar CMOS stacked, currently the stack height is 3.
  - There will be more complex counters, some polling of adjacent pixels to try to account for split-pixel events, some forms of MCA (energy resolving, multi-channel analyzer) functionality pixel-by-pixel.
  - There will be variations of analog and digital storage of information inside the PAD. The circuits are so similar at times that words fail to distinguish.
  - Larger arrays will be made mostly by silicon-on-insulator processes.
  - It is interesting to note that a complete, small PAD array, say 32 x 32, 1 mm area, might cost about $130K for a prototype development today. Again one can forecast the coming of niche chips.
  - It is also interesting to note that ASIC amplifiers have noise 10-100 times lower than printed circuit board based ones – lower capacitance, better packing, the future belongs to the IC.
  - PAD arrays will be tried with "time slicing" protein crystallography – no shutter, fast motor rotation. Crystallographers will also be brought on board by expanded digital logic / pixel.
- **Avalanche Photodiode Arrays** [50 ns to 500 ps]
  - An ESRF, DESY development of arrays for timing applications will become available. An emphasis here is on in-elastic scattering applications, measuring the time duration between x-rays.
  - There can be avalanche photo diode arrays responding in the100-500 ps range.
- **Picosecond level detectors** [500 ps to 5 ps] will start to appear in research format.

    - It is straight forward to see a path to 500-100 ps count times, and it is conceivable to see 10 ps count times.
    - Propagation delay thru a logic gate, 0.11 um, (110 nm) feature size is 25 ps [Ref: foundry], and this number scales linearly with feature size reduction. Hence 45 nm features, about 12 ps delay.
    - There will be niche applications of fast response photoconductors, perhaps modified by neutron damage, or by insertion of spoiler dopants such as gold.
    - There will intense interaction in this area with other technology areas, for example microwave engineering. We will see a shortage of microwave engineers.
    - There will be research into <10ps count times by groups that can work directly with modern foundries.
    - There will continue to be research in ballistic (no scattering by carriers) transport inside nano-sized devices. These can be ps-fast.
    - There will be growing connection with nano-technologies in general.
- **Amorphous silicon** array [0.1 sec to 0.01 sec] performance will improve very modestly or perhaps not at all.
    - The charge trapping, image lag issue is inherent in the material. Perhaps there will be some push for direct detection. On the other hand, they will be more commercially available, and thus exist, and serve needs on beamlines.
    - Organic film transistor arrays will begin to appear at the research level, competing for the same niche. They are slow, and noisy, but cheap and will be sprayed on like ink. Detectors can ride the wave of electronic-folding-paper.
    - Somebody might produce a detector that conforms to the inside of a 2 m sphere.
- There will be increased integration of detector technology **with x-ray optics** (multi-layers, energy dispersive gratings, etc). Fast detectors are electronically noisy detectors, so cannot have good energy resolution.
- **Micro channel plate** detectors [1us] will continue to have niches in fast framing. It seems that image intensifiers are pretty much gone the way of film.
- There will be modest pushes for **signal processing** – FPGA's to compress the data and so-forth. In general however, beamlines seem to like to have the "raw" data. This will be seen to be more and more impractical.
    - Programming an FPGA is about 1/10 as efficient (time-wise) as programming in C-code.
    - Software tools and libraries are expensive, but synergistic with demands of controls groups.
- I doubt much will be done **with superconducting detectors**, [1ms to 10 us] transition edge sensors etc, applied to the APS in next 5 years. Their count rates are very low, and they only exist in specialized labs (and at the ALS).

One can predict how the work will be done:

- Most successful projects will involve industry. We will feel the need to train people to work as contracts managers.
- Synergy with x-ray medical imaging will remain a hoped for, but never-quite-realized goal, as has been the case for the past 15 years.
- Collaborations with other national labs will be advocated, but will generally fail because we see each other as competitors for scarce DOE funds.

- The main source of original information will be semiconductor foundries.
- Given funding, detector development will continue to ride the wave of the semiconductor industry, the largest and most vibrant industry on earth, which has produced almost miraculous improvements. If you want to understand detectors, understand as well this foundation technology.
  - For example, I now have a 32 GB memory stick – 2 years ago it was 64 MB. Some interesting scaling:
  - Per the textbooks, the power of an IC scales with the cube of the feature size, so dropping the size of a transistor by ½ reduces the power to 1/8. Power is typically a worry, or a limit, with dense, fast circuitry.
  - The scale size of transistors drops by ½ every 18 months, and is now at 45 nm for commercial IC's at, say IBM. To keep this scaling law going, people will turn to 3-D CMOS. Google 3-D CMOS.
  - Transistors must be modeled to be used:
    - Transistors larger than 2 um conform to simple parameterization, called SPICE level 3, about 20 free parameters.
    - Smaller than 0.5 um, the transistor must be treated as a 2 or 3-D structure. But typically this is fudged, and the empirical models for transistors now have some 150 free parameters. Obviously there is an intense push to get the models correct, but analog lags digital.
    - With digital electronics, speed is the most important, with analog electronics predictability is the most important, even if speed is lowered. (Ref: IBM foundry person, at HEP conference.)
  - The scale size of the transistor seems to be the largest determinant of the cost of the wafer run, the mask set, etc.
    - Currently this cost rises quickly below 0.25 um. (Ref: MOSIS)
    - There will come a day when mask sets are not required, and the semiconductor pattern is raster scanned on. The mask cost will disappear. (Ref: work at Bell Labs etc….)
  - The unity gain frequency of transistors is expected to approach 1 THz in coming years. This is the frequency up to which a transistor can provide gain. (Ref Stanford SOI short course) Germanium doped silicon bipolar transistors are in this range, I am not that knowledgeable about III-V transistors, but obviously GaAs or InP are fast.
  - The HEP community is very interested in fast electronics, for example Analog to Digital conversion at speeds > 5 GSamp / sec. The aerospace community is also, but has a bigger budget. One sees them working with III-V compounds such as InP, with perhaps 10 GSamp/sec. (Ref: NGC Corp)
  - CERN people know a lot more about radiation damage; I am pretty ignorant here other than to know that oxide charging damage rates drop as feature sizes drop below 0.25 um.
  - Per foundry people, there is no substitute for prototyping, and trying it out.
- Most of the development work will be done in Europe.
  - The delay time before the instrumentation comes to the APS will be inversely proportional to the detector's speed. (Faster detectors are harder to integrate into beamlines.)